FPGA Design Engineer

Everspin Technologies has an immediate opening for a highly motivated, success-oriented, experienced Digital Design Engineer working in the Systems Development group.

Scope of Responsibility/Expectations

Digital Design/RTL Developer responsible for FPGA design flow including specification, RTL design, logic synthesis, verification, timing analysis, and more. Engineer will be expected to define and implement project plans, manage milestones, and hold peer reviews to ensure readiness for product release. Ideal candidate must be able to work independently as well as with a cross functional team. Good communication skills and strong team work is required. Opportunity is in our Austin based design center.

Desired Skills and Experience

- Experience in FPGA design and development using verilog, FPGA simulation, FPGA design verification using verification and debugging tools.
- Knowledge of FPGA constraints leading to timing closure in FPGA routes.
- Experienced using lab test equipment such as oscilloscopes and logic analyzers
- Understanding standard memory interface protocols such as DDR3 and DDR4.
- Experience with FPGA design using Verilog and with EDA tools such as Modelsim, Cadence Incisive, Xilinx ISE/Vivado and Altera Quartus

Education and Experience

BS in electrical engineering, computer engineering, or equivalent education and experience, is required. A track record of innovation and leading-edge expertise is expected in the relevant areas.

The Company

Everspin Technologies is the world's first volume MRAM supplier and continues to lead the industry by advancing the technology and expanding its MRAM product portfolio. The open position is at the Austin Design Center and not at the company headquarters located in Chandler, Arizona (greater Phoenix metropolitan area). It is a salaried position that includes benefits including: medical, dental, vision plan, paid time off, and a 401k retirement plan.

Contact

Please send resume to jobs@everspin.com